U.S. Patent Application Serial No. 10/756,763

Response dated May 1, 2007

Reply to OA of February 2, 2007

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-12. (Canceled)

Claim 13 (Previously Presented): An electronic parts packaging structure comprising:

a wiring substrate including a wiring pattern;

a first insulation film formed on the wiring substrate;

an electronic parts having a connection terminal on an element formation surface, the

electronic parts being buried in the first insulation film in a state where the connection terminal is

directed upward and being mounted in a state where a lower portion of the first insulating film exists

between the electronic parts and the wiring substrate, and the back side of the electronic parts is

electrically insulated with the wiring substrate by the lower portion of the first insulation film;

a second insulation film for covering the electronic parts, and whose upper surface is flat over

a whole on the wiring substrate, and the second insulation film contacting with the electronic parts

as a single layer, and;

first via holes formed in a predetermined portion of the first and second insulation films on

the wiring pattern, and having an identical inner surface;

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second via holes formed in a portion of the second insulating film on the connection terminal

of the electron parts;

via holes respectively formed in a predetermined portion of the first and second insulation

films on the wiring pattern and the connection terminal;

an upper wiring pattern as a single wiring formed on the second insulation film, the upper

wiring pattern being connected to the wiring pattern and the connection terminal through the via

holes, wherein, the electronic parts is electrically connected to the wiring pattern of the wiring

substrate by only the upper wiring pattern; and

an upper electronic part whose bumps are flip-chip bonded to connection portions of the

upper wiring pattern, the connection pad which directly contacts the upper surface of the second

insulating film.

Claim 14. (Canceled)

Claim 15 (Currently Amended): The electronic parts packaging structure according to

claims 13 or 14 claim 13, wherein the element formation surface of the electronic parts and an upper

surface of the insulation film in which the electronic parts is buried are at an almost same height to

be planarized.

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Claim 16 (Currently Amended): The electronic parts packaging structure according to claims 13 or 14 claim 13, wherein the electronic parts is a semiconductor chip having a thickness of approximately 150 μ m or less.

Claim 17 (Currently Amended): The electronic parts packaging structure according to claims 13 or 14 claim 13, wherein the insulation film is made of resin.